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RTXcore ver 1.0

25 September 2006

Technical

Introduction

The RTXcore is a logical replacement for the RTX2000 microprocessor intended for implementation on an FPGA. On a Xilinx Spartan XC2S300E RTXcore runs at twice the rate of the original processor and supports the complete documented instruction set as well as the timers and interrupt logic built into the RTX2000. Forth and C compilers are available from MicroProcessor Engineering and other vendors.

Description

The RTXcore core replicates the functional behaviour of the RTX2000 microprocessor as described in documents available in the public domain. The RTXcore includes all the signal pins of the RTX2000 and duplicates the documented behaviour of all active signals on a cycle by cycle basis.

The RTXcore targets the Xilinx Spartan 2E, Virtex and Virtex E families of FPGAs. The source for the core is written in VHDL and has been synthesised using the Xilinx ISE 5.1.03i synthesis and PAR software. The core uses three block RAMs and about 70% of the slices in a XCV300E. It has been implemented and tested on boards containing both Spartan 300E and Virtex 300 FPGAs. Porting to other FPGAs including Actel rad-hard devices can be arranged.

The internal timing supports an ICLK of up to 40 MHz depending on FPGA and speed grade. No attempt has been made to mimic the RTX2000 external timing specifications. External timing will be dependent on each users implementation. It is expected that the user will adjust their I/O design to meet their requirements considering the achieved timing of the core at the required ICLK frequency on the selected FPGA.

The RTX2000 source documents used are as follows:

- Harris RTX-2000 Programmer's Reference Manual
- The RTX-2000 Hardware Reference Manual

Logical testing of the core has included cycle by cycle comparisons with a physical RTX2000 while executing a suite of programs. These programs exercised the instruction set as well as the timer and interrupt logic. The cycle by cycle comparisons verified that the core produced the same output from active outputs as the real RTX2000.

Deliverables

Design information is supplied on CD and includes the following:

- Source files
- Simulation project files
- Timing project files targeting Virtex and Virtex E devices

The source files for the RTXcore consists of the following VHDL files:

- top_bram_stk.vhd
- idecode.vhd
- interrupt_controller.vhd
- timer.vhd

Top_bram_stk.vhd describes the main data paths, registers and ALU. Idecode.vhd is combinatorial logic performing instruction decoding. Interrupt_controller.vhd includes the logic for processing interrupt. The design uses a single clock, ICLK from which PCLK and TCLK are generated. The core is provided with separate input and output ports for both the memory bus and G bus. This arrangement is useful for interfacing to additional I/O devices located in the FPGA. An additional top level VHDL file is included to multiplex the input and output memory and G buses into single bi-directional buses.

The simulation project is a complete simulation of the RTXcore with RAM. The RAM is initialised with an image of the MPE Forth interpreter. The testbench repeatedly sends Forth instructions to the interpreter and displays the text output from the RTXcore on the simulator console. The simulation project is for the ModelSim XEII v5.6e VHDL simulator available with the Xilinx Webpack tools from www.xilinx.com.

The timing projects provide synthesis and PAR results when targeting the Virtex and Virtex E FPGAs. The projects include the multi-cycle timing constraints required to meet an ICLK of 20 MHz for the Virtex and 40 MHz for the Virtex E parts.

The VHDL component declaration for the core is as follows:

```
COMPONENT xrtx
      PORT(
            pINTSUP : IN std_logic;
            pNMI : IN std_logic;
            pEI1 : IN std_logic;
            pEI2 : IN std_logic;
            pEI3 : IN std_logic;
            pEI4 : IN std_logic;
            pEI5 : IN std_logic;
            pICLK : IN std_logic;
            pWAIT : IN std_logic;
            pRESET : IN std_logic;
            pMA : OUT std_logic_vector(18 downto 0);
            pMD : IN std_logic_vector(15 downto 0);
            pMDout : OUT std_logic_vector(15 downto 0);
            pGD : IN std_logic_vector(15 downto 0);
```

```
            pGDout : OUT std_logic_vector(15 downto 0);
            pPCLK : INOUT std_logic;
            pTCLK : INOUT std_logic;
            pUDS : OUT std_logic;
            pLDS : OUT std_logic;
            pNEW : OUT std_logic;
            pBOOT : OUT std_logic;
            pMR : OUT std_logic;
            pGR : OUT std_logic;
            pNGIO : OUT std_logic;
            pGA : OUT std_logic_vector(2 downto 0);
            pINTA : OUT std_logic
            );
END COMPONENT;
```

Evaluation board

The default evaluation board is the Xilinx S3 development board from the Spartan-3 starter kit. Please contact MPE for further details.

Commercial

The full core deliverables are available for:
GBP 25,000 EU ~36,250 USD ~47,000
The VHDL code will only be delivered after signature of a Non Disclosure Agreement. The license terms are for one working group, and the license is not transferable without agreement from MPE. The RTXcore may not be used for Magnetic Resonance Imaging (MRI) purposes. The license text is very similar to our Source code NDA.

The package includes technical support by phone, fax and email. Additional support contracts are available based on a day rate of GBP 1,000 per 8 hour day. An annual extended technical support contract is available which includes all VHDL upgrades and application level support.

Software development

Forth5 Compiler for the RTX2000/2010

Details of this compiler are available from the Forth 5 section of the MPE web site at:
http://www.mpeforth.com/forth5.htm

Price (GB Pounds) £2,495

ANSI C compiler for RTX 2000/2010 processors, Part no. VFXCRTX

The MPE VFX C for the RTX family supports the full address space of the CPU using a large memory model so that both code and data can occupy the available 1Mb address space. The code generation quality is better than that of the small model compiler for the RTX from other suppliers. A copy of the manual is available on request or from our website at:
http://www.mpeforth.com/rtx.htm
Price (GB Pounds) £4,450

RTX core FAQ

The following are extracted for conversations with clients.

> What versions are available:
We are not (yet) selling silicon. What we are selling is VHDL source code that the user puts into FPGAs. There are rad-hard FPGAs available from Xilinx and Actel.

> I know you mentioned there will be a full Rad Hard space version,
> but will there be lower cost non RH / RT equivalents to the
> /proto, with 883 temperature range, and will there be a proper
> 883 version?
The standard VHDL is targeted to Xilinx Spartan and Virtex commercial FPGAs. Evaluation of the RTXcore can be performed on the Xilinx S3 starter board.

Please contact MPE for price and delivery information for ports to other FPGAs.

> What package does the FPGA come in?
Commercial parts are TQFP. For rad-hard parts, see the Xilinx and Actel data sheets.

> We want CQFP (ceramic quad flat pack) to match the original
> Intersil part. Will it be drop in pin for pin compatible?
Most unlikely! However, we can design adapters from virtually any pinout to the PGA 84/85 pinout of the original RTX20xx family. However, the RTX20xx devices ran at 5v, and the devices we have used so far are 3.3v devices.

> What is the price for VHDL source?
The price for the VHDL sources is GBP 25,000. This includes everything you need, the RTXcore code, all the RTX peripherals plus a UART. The code is compilable using the Xilinx Web Pack.

> I believe the (now obsolete) Intersil RH RTX2010 was approx USD
> 4000 each. We have just bought large quantities of this and
> realise the stocks are virtually depleted, hence they are so
> interested in your FPGA compatible device.
I expect that they will have to modify their hardware, but
1) it will be cheaper
2) it will be faster
3) they can put additional peripherals into the FPGA.

> The customer is interested in putting the RTX core on the Actel
> RTAX2000S. Any idea if it's compatible? A Xilinx-only solution
> would not be acceptable to them.
The implementation makes use of the Xilinx block RAM. This will need to be changed to whatever is available on Actel parts. Some notes follow below. On the Xilinx tools you can run Forth on the VHDL simulator! We didn't have to change anything in the Forth or C compilers. We can arrange a port to the Actel devices.

Suppliers and Agents

All orders for delivery to India must be received by MPE from the UK office of Spur Electron. Purchase departments requiring delivery to India should contact:

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